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an overlap region of the oxide layer located beneath said gate structure and adjacent said first leading edge and inward of said second leading edge, said overlap region having a predetermined ion implant concentration higher than in remaining oxide layer portions adjacent both sides of said overlap region, said predetermined implant concentration being sufficient to increase the electrical gate oxide thickness in said overlap region.

2. (Original) The circuit structure according to claim 1, wherein said predetermined ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

3. (Currently Amended) A circuit structure comprising:

a semiconductor layer;

a source region and a drain region in said semiconductor layer which are lightly doped with a first conductivity-type dopant;

a channel region located between said source/drain regions;

a gate oxide layer located on a surface of said channel region; and

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a gate electrode located on said gate oxide layer, wherein a portion of said gate oxide layer defines an overlap region, which is beneath said gate electrode inward of said source region and adjacent said drain region, said overlap region having an ion implant concentration higher than in remaining portions of said oxide layer adjacent both sides of the overlap region, which is effective to lower the surface electrical field in said overlap region.

4. (Original) The circuit structure according to claim 3, wherein said ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

5. (Original) The circuit structure according to claim 3, wherein said source region and said drain region are heavily doped with a second conductivity dopant.

6. (Currently Amended) The circuit structure according to claim 3, further including a pair of spacers adjacent said gate electrode.

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7. (Original) The circuit structure according to claim 3, wherein said gate electrode is comprised of polysilicon.

8. (Original) The circuit structure according to claim 3, wherein said gate electrode is a gate stack.

9. (Original) The circuit structure according to claim 3, wherein said gate electrode is comprised of a layer of polysilicon, and one or more additional layers selected from the group consisting of metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks).

10. (Previously Amended) The circuit structure according to claim 3, wherein said gate electrode is comprised of a layer of polysilicon, a layer of titanium nitride deposited on said polysilicon layer, and a layer of tungsten deposited on said titanium nitride layer.

11. (Original) The circuit structure according to claim 3, further including a pair of conductive studs and an interlevel dielectric layer provided on said semiconductive layer, said interlevel dielectric layer have a pair of throughbores, each accommodating one of each said pair of conductive studs, and one of each said pair of conductive studs contacting one of each said source/drain regions.

12. (Currently Amended) A circuit structure comprising:

a semiconductor layer;

a first dopant-type MOS transistor is situated on said semiconductor layer having:

a source region and a drain region in said semiconductor layer which are doped with a first conductivity-type dopant;

a channel region located between said source/drain regions;

a gate oxide layer located on a surface of said channel region; and

a gate electrode located on said gate oxide layer, wherein a portion of said gate oxide layer defines an overlap region, which is beneath said gate electrode inward of said source region and adjacent said drain region, said overlap region having an ion implant concentration

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higher than in remaining portions of said gate oxide layer adjacent both sides of the overlap region, which is effective to lower the surface electrical field in said overlap region; and,

a second-type dopant MOS transistor which is complementary to said first dopant-type MOS transistor, said second-type dopant MOS transistor is situated on said semiconductor layer and includes a second gate oxide layer, two complementary source/drain regions which are doped with a second conductivity-type dopant, and a complementary gate electrode located on said second gate oxide layer.

13. (Original) The circuit structure according to claim 12, wherein said ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

14. (Previously Amended) The circuit structure according to claim 12, wherein a portion of said second gate oxide layer which is beneath said complimentary gate electrode and adjacent said complimentary drain region, and which defines a second overlap region, having an ion implant concentration which is effective to lower the surface electrical field in said second overlap region.

45. (Currently Amended) A circuit structure comprising:

a semiconductor layer having a source region, a drain region, and a channel region located between said source/drain regions;

a gate oxide layer located at least on a surface of said channel region; and

a gate electrode located on said gate oxide layer, wherein a first portion of said gate oxide layer beneath said gate electrode and adjacent said drain region has a higher ion implant concentration than in remaining portions of said gate oxide layer adjacent both sides of said first portion.

46. (Original) The circuit structure according to claim 45, wherein said ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.